

PATENT 4450-0316P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant:

Howard H. IRELAND et al. Conf.:

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2133

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For:

METHOD AND APPARATUS FOR GENERATING BIT ERRORS IN A FORWARD ERROR CORRECTION

(FEC) SYSTEM TO ESTIMATE POWER

DISSIPATION CHARACTERISTICS OF THE

SYSTEM

RECEIVED

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Technology Center 2100 March 1, 2004

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

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Respectfully submitted,

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